Ph.D. Position: Rethinking LDPC codes and decoders to minimize decoding energy

Summary

Research area:	Mainly information theory and optimization, with some cross-disciplinary considerations for computer architecture and VLSI circuit design.
Supervisors:	Dr. Elsa Dupraz (elsa.dupraz@imt-atlantique.fr) Dr. François Leduc-Primeau (francois.leduc-primeau@imt-atlantique.fr)
Director:	Dr. Frédéric Guilloud (frederic.guilloud@imt-atlantique.fr)
Start date:	Ideally, October 2017, no later than December 2017
Funding:	ANR project EF-FECtive. Fully funded Ph.D. including salary for 3 years, travel to conferences, and personal computer.
Institution:	IMT Atlantique, located in Brest, France.

Context of the Work

Error-correction codes (ECCs) such as LDPC and Turbo Codes are used in the vast majority of communication systems because they allow a large reduction of the transmitter power. However, the capabilities of codes used in practical systems are often limited by the energy consumption of the decoding circuit. Energy consumption is seen as a critical aspect in the ongoing 5G standardization process which targets an important increase in battery lifetime and a reduced environmental footprint. As a result, optimizing the trade-off of coding gain versus decoding energy will be fundamental for the channel codes used in the next generations of telecommunication systems.

The importance of optimizing the energy consumption is further compounded by the great difficulty being faced today in improving the energy efficiency of VLSI circuits. Whereas in the past reducing the feature size enabled a reduction of the supply voltage, and in turn of the energy per operation, this is no longer the case for current process technologies. One approach that enables a continued progression of energy efficiency is to operate circuits in the *near-threshold* regime, where the supply voltage is approximately the same as the threshold voltage of the transistors. Near-threshold circuits can provide a 10× improvement in energy efficiency [1], but unfortunately it is difficult to operate such circuits reliably at full speed. One current major challenge of energy efficiency in telecommunication systems is thus to design highly reliable error correction systems on near-threshold circuits.

Objectives

The objective of the Ph.D. is to develop the theoretical framework and the technical solutions that will permit to design powerful LDPC codes for energy-efficient hardware implementations. The project plans to develop and fabricate an ASIC circuit of an LDPC decoder that will operate in the near-threshold regime (realized by an ASIC engineer hired by the project). This circuit will be used to assist in the construction of theoretical models of energy consumption, and to demonstrate the theoretical findings at the end of the project.

The Ph.D. student will work in close collaboration with the engineer in order to derive energy models that are both accurate and suitable for the design of powerful and energy-efficient LDPC codes and decoders, and will develop methods to optimize the LDPC code constructions and particular aspects of the decoder in order to minimize energy. The ultimate goal of the research is to decrease the energy consumption of LDPC decoders by 10× by allowing them to tolerate faults that occur

within the decoder. To achieve this, we will be taking advantage of the group's extensive experience on LDPC decoders and fault-tolerant implementations [2–6].

Laboratory and Funding

The work will be carried out in the Signal & Communication department of IMT Atlantique, Brest, France, under the supervision of Dr. Elsa Dupraz, with the co-supervision of Dr. François Leduc-Primeau. IMT Atlantique is recognized for its many achievements in the area of channel coding, starting with the invention of Turbo codes in 1993. This project is supported by a grant from Agence Nationale de la Recherche (ANR). In addition to the full funding of the Ph.D. student, the grant includes several additional resources, such as the collaboration of an ASIC engineer and the fabrication of an ASIC circuit. The Ph.D. student may also have opportunities for visits to foreign labs (funded by the project), especially in Montreal, Canada.

Candidate Profile

The successful candidate should have a solid academic background in telecommunications and signal processing, including a good knowledge of information theory and/or error-correction codes. She/He should demonstrate good programming skills. A prior experience with either LDPC codes or hardware design would be a plus.

How to Apply

Send an e-mail to elsa.dupraz@imt-atlantique.fr and francois.leduc-primeau@imt-atlantique.fr with the subject line "EF-FECtive PhD position", including a full CV, university transcripts, recommendation letters or contacts from former teachers/advisors, and a statement (max. 1 page) describing how your experience prepares you for this project.

References

[1] R. Dreslinski, M. Wieckowski, D. Blaauw, D. Sylvester, and T. Mudge, "Near-threshold computing: Reclaiming Moore's law through energy efficient integrated circuits," *Proc. of the IEEE*, vol. 98, no. 2, pp. 253–266, Feb. 2010.

[2] F. Leduc-Primeau and W. J. Gross, "Faulty Gallager-B decoding with optimal message repetition," in *Proceedings of the 50th Allerton Conference on Communication, Control, and Computing*, Oct. 2012.

[3] F. Leduc-Primeau, F. R. Kschischang, and W. J. Gross, "Modeling and energy optimization of LDPC decoder circuits with timing violations," *CoRR*, vol. abs/1503.03880, 2015. [Online]. Available: http://arxiv.org/abs/1503.03880

[4] F. Leduc-Primeau and W. J. Gross, "Finite-length quasi-synchronous LDPC decoders," in *9th Int. Symp. on Turbo Codes and Iterative Information Processing*, Sep. 2016, pp. 325–329.

[5] E. Dupraz, D. Declercq, B. Vasic, and V. Savin, "Analysis and design of finite alphabet iterative decoders robust to faulty hardware," *IEEE Transactions on Communications*, vol. 63, no. 8, pp. 2797–2809, Aug. 2015.

[6] E. Dupraz, D. Declercq, and B. Vasic, "Asymptotic error probability of the gallager B decoder under timing errors," *IEEE Communications Letters*, 2017.