Memory Efficient APP Decoding of LDPC Codes

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Abstract

We propose memory efficient parallel and serial a posteriori probability (APP) decoders. They require memory that is linear in the number of nodes in the Tanner graph of the code. For high-rate codes this is a significant saving compared to the existing iterative decoders, which require memory that is at least proportional to the number of edges. We present a framework for theoretical analysis of the decoders and show that the serial version converges faster that the parallel one.

Key words: BP decoder, APP decoder, LDPC, memory complexity, error probability analysis

1 Introduction

Belief propagation (BP) is an iterative message-passing algorithm for decoding low density parity check (LDPC) codes [2], widely used in many systems. Despite its good error correction performances and capability of approaching the Shannon limit, BP suffers from large memory requirements for message processing and storage, proportional to the number of edges in the Tanner graph of the code [7]. Such large memory requirements coupled with additional hardware resources needed for the message updating make the BP less attractive in applications with stringing constraints on decoding throughput and code rate.

A posteriori probability (APP) decoder [1] is a suboptimal alternative to BP, in which the variable node processing is simplified by allowing variables to send messages in an intrinsic manner, and a message from a variable node corresponds to a posteriori value used to estimate that variable. While overall computational savings introduced by the APP decoder are not significant, as the BP variable node processing is already simple, the computations can be realized in a memory efficient way.

We propose two memory-efficient versions of APP decoder based on parallel scheduling [3] and serial scheduling [9], [5] schemes, previously considered for BP decoders. They both require memory proportional to the number of nodes in the Tanner graph of the LDPC code, rather than to the number of edges, as proposed in [1]. We consider

the theoretical analysis for the parallel APP decoder proposed in [6], and adapt it to the case of serial scheduling. According to our theoretical analysis, we show that, for a small number of iterations, serial scheduling enables to achieve a lower level of error probability than parallel scheduling.

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References

[1] M.P.C. Fossorier, M. Mihaljević, and H. Imai. Reduced complexity iterative decoding of low-density parity check codes based on belief propagation. *Communications, IEEE Transactions on*, 47(5):673–680, May 1999.

[2] R. G. Gallager. *Low Density Parity Check Codes*. M.I.T. Press, Cambridge, MA, 1963.

[3] F. Guilloud, E. Boutillon, J. Tousch, and J.-L. Danger. Generic description and synthesis of ldpc decoders. *Communications, IEEE Transactions on*, 55(11):2084–2091, Nov 2007.

[4] Kevin Karplus and Habib Krit. A semi-systolic decoder for the pdsc-73 error-correcting code. *Discrete Applied Mathematics*, 33(1–3):109 – 128, 1991.

[5] Haggai Kfir and Ido Kanter. Parallel versus sequential updating for belief propagation decoding. *Physica A: Statistical Mechanics and its Applications*, 330(1–2):259–270, 2003.

[6] M.J. Mihaljevic and J.D. Golic. A method for convergence analysis of iterative probabilistic decoding. *Information Theory, IEEE Transactions on*, 46(6):2206–2211, Sep 2000.

[7] R. M. Tanner. A recursive approach to low complexity codes. *IEEE Trans. Inf. Theory*, 27(5):533–547, May 1981.

[8] E. Yeo, P. Pakzad, B. Nikolic, and V. Anantharam. High throughput low-density parity-check decoder architectures. In *Proc. of Global Telecommunications Conference, 2001. GLOBECOM '01. IEEE*, volume 5, pages 3019–3024 vol.5, 2001.

[9] Juntan Zhang and M. Fossorier. Shuffled belief propagation decoding. In *Signals, Systems and Computers, 2002. Conference Record of the Thirty-Sixth Asilomar Conference on*, volume 1, pages 8–15 vol.1, Nov 2002.